Errata Sheet and Guidelines for MAX 10 ES Devices

ES-1040
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Device Errata for MAX 10 ES Devices

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This errata sheet provides information about known device issues affecting MAX® 10 engineering sample (ES) devices.

Note:
- ES devices are not intended to be used for volume production or device qualification testing.
- ES devices are intended to be used at nominal voltage and nominal temperature only for DDR3 external memory interface (EMIF) support.

Table 1-1: Device Errata for MAX 10 ES Devices

This table lists the specific device issues and the affected MAX 10 ES devices.

Issue	Affected Devices	Planned Fix
ADC Prescalar on page 1-1 • ADC prescalar gain error • ADC prescalar THD performance	10M08 ES	Production Devices
ESD Performance on page 1-2 HBM ESD performance for MAX 10 ES devices is below target level	10M08 ES	Production Devices
Timing Model Adjustment on page 1-2 Timing model adjustment on I/O-to-Core and Core-to-I/O for MAX 10 ES devices	10M08 ES	Updated Timing Model in the Quartus II software version 15.0

ADC Prescalar

The ADC prescalar in the 10M08 ES devices does not meet datasheet specifications, affecting gain error and total harmonic distortion (THD) specifications. Other specifications related to prescalar are not affected. This issue will be fixed in production devices.

Table 1-2: Gain Error and Drift Specifications for 10M08 ES Devices

Parameter	Symbol	Condition	Channel	Min	Typ	Max	Unit
Gain error and drift	Egain	With prescalar on	8	2	—	5	%FS
		With prescalar on	16	–1	—	1	%FS

Table 1-3: Total Harmonic Distortion Specifications for 10M08 ES Devices

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Total Harmonic Distortion	THD	F_{IN} = 50 kHz, F_S = 1 MHz, PLL, Prescalar enabled	61	—	—	dB

ESD Performance

HBM ESD performance for 10M08 ES devices is below target levels (CDM meets targets). Altera will improve ESD performance in production devices.

As per JEDEC document JESD625b, follow the standard ESD handling guidelines, particularly for human handling, (i.e. wear proper ground strap) when handling 10M08 ES devices.

Timing Model Adjustment

To better align the Quartus® II timing models with silicon characterization, Altera recommends adjusting the timing for I/O-to-Core and Core-to-I/O data transfer in MAX 10 ES devices. For temporary solution, add 300 ps (0.3 ns) clock uncertainty in TimeQuest Timing Analyzer.

To add 300 ps (0.3 ns) clock uncertainty in TimeQuest Timing Analyzer, add the following constraints in the Synopsys Design Constraints File (**.sdc**):

- `set_clock_uncertainty –setup –to <clock name> -setup –add 0.3`
- `set_clock_uncertainty –hold –enable_same_physical_edge –to <clock name> –add 0.3`

For example:

```
set_clock_uncertainty -to { inst|altpll_component|auto_generated|pll1|
clk[1] } -setup 0.3
```

After adding the **.sdc** file constraint, a clock uncertainty row is added in **Data Required Path** in the timing report.

Figure 1-1: Timing Report Before 300 ps Clock Uncertainty is Added

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	0.486	datain_deg90	deg90_reg	virclk	inst|altpll_component|auto_generated|pll1|clk[1]	2.500	-0.021	1.369

	Total	Incr	RF	Type	Fanout	Location	Element
15	1.217	0.000	RR	IC	1	CLKCTRL_G4	inst|altpll_component|auto_generated|wire_pll1_clk[1]~clkctrl|inclk[0]
16	1.217	0.000	RR	CELL	1	CLKCTRL_G4	inst|altpll_component|auto_generated|wire_pll1_clk[1]~clkctrl|outclk
17	1.217	0.000		RE	1	CLKCTRL_G4	CUDA_CLKBUF
18	1.227	0.010		RE	1	CLKBUF_OUT_X0_Y9_N32_I0	CLKBUF_OUT
19	1.381	0.154		RE	1	GLOBAL_CLK_H_X0_Y9_N0_I4	GLOBAL_CLK_H
20	1.494	0.113		RE	1	GLOBAL_CLK_V_X10_Y10_N0_I4	GLOBAL_CLK_V
21	1.645	0.151		RE	1	SCLK_TO_ROWCLK_BUF_X10_Y20_N0_I14	SCLK_TO_ROWCLK_BUF
22	2.056	0.411		RE	1	LAB_CLK_X11_Y20_N0_I5	LAB_CLK
23	2.120	0.064		RE	1	BLK_CLK_BUF_X31_Y20_N0_I5	BLK_CLK_BUF
24	2.118	-0.002	RR	IC	1	FF_X31_Y20_N17	deg90_reg|clk
25	2.479	0.361	RR	CELL	1	FF_X31_Y20_N17	deg90_reg
3	2.355	-0.124		uTsu	1	FF_X31_Y20_N17	deg90_reg

Figure 1-2: Timing Report After 300 ps Clock Uncertainty is Added

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	0.186	datain_deg90	deg90_reg	virclk	inst|altpll_component|auto_generated|pll1|clk[1]	2.500	-0.021	1.369

Data Required Path

	Total	Incr	RF	Type	Fanout	Location	Element
16	1.217	0.000	RR	CELL	1	CLKCTRL_G4	inst|altpll_component|auto_generated|wire_pll1_clk[1]~clkctrl|outclk
17	1.217	0.000		RE	1	CLKCTRL_G4	CUDA_CLKBUF
18	1.227	0.010		RE	1	CLKBUF_OUT_X0_Y9_N32_I0	CLKBUF_OUT
19	1.381	0.154		RE	1	GLOBAL_CLK_H_X0_Y9_N0_I4	GLOBAL_CLK_H
20	1.494	0.113		RE	1	GLOBAL_CLK_V_X10_Y10_N0_I4	GLOBAL_CLK_V
21	1.645	0.151		RE	1	SCLK_TO_ROWCLK_BUF_X10_Y20_N0_I14	SCLK_TO_ROWCLK_BUF
22	2.056	0.411		RE	1	LAB_CLK_X11_Y20_N0_I5	LAB_CLK
23	2.120	0.064		RE	1	BLK_CLK_BUF_X31_Y20_N0_I5	BLK_CLK_BUF
24	2.118	-0.002	RR	IC	1	FF_X31_Y20_N17	deg90_reg|clk
25	2.479	0.361	RR	CELL	1	FF_X31_Y20_N17	deg90_reg
3	2.179	-0.300					clock uncertainty
4	2.055	-0.124		uTsu	1	FF_X31_Y20_N17	deg90_reg

Device Guidelines for MAX 10 ES Devices

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This guidelines sheet provides Altera's recommended guidelines when using MAX 10 ES devices.

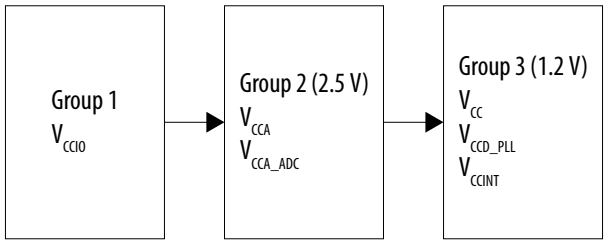
Note:
- ES devices are not intended to be used for volume production or device qualification testing.
- ES devices are intended to be used at nominal voltage and nominal temperature only for DDR3 EMIF support.

Recommended Power-up Sequencing for MAX 10 ES Devices

To ensure the minimum current draw during power up and configuration for MAX 10 dual supply ES devices, follow the recommended power-up sequence as shown in the figure below.

Figure 2-1: Recommended Power-up Sequence

The power rails in each group must be ramped up to a minimum of 90% of their full rail before the next group starts.



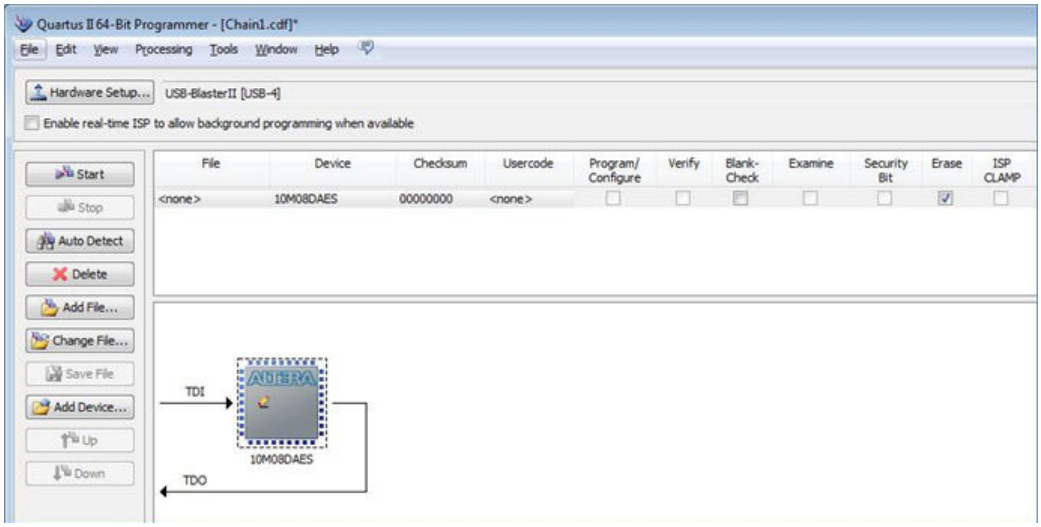
Full Chip Erase Prior to Initial Device Programming

You must perform a full chip erase prior to device programming when you use the MAX 10 device for the first time. The full chip erase prevents the reconfiguration watchdog timer from timing out. The full chip erase must be done only prior to initial programming.

For full chip erase, follow these steps:

1. Open the Quartus II Programmer.
2. In the **Programmer** window, click **Hardware Setup** and select **USB Blaster**.
3. Click **Auto Detect** on the left pane.
4. Select the device and set the **Erase** column as shown in the following figure.
5. Click **Start** to start full chip erase.

Figure 2-2: The Quartus II Programmer



Migration Guidelines

This migration guidelines is applicable if you plan to use MAX 10 SC or SF variant (for single supply devices) and DC or DF variant (for dual supply devices) in production devices.

Altera recommends designing your board with MAX 10 ES device SA or DA variant according to the recommendation for SC or SF variant (for single supply devices) and DC or DF variant (for dual supply devices). There are cross variants pin mismatches between MAX 10 ES devices and MAX 10 production devices. You can migrate the pins as recommended in the following tables without impact to your design.

Table 2-1: MAX 10 Devices Migration from ES Device SA Variant to Production Device SC or SF Variant

MAX 10 ES Device SA Variant Pin	MAX 10 Production Device SC or SF Variant Pin
ADC_VREF	VCCA
ANAIN1	GND
REFGND	GND
ADC1IN[1..8]	I/O

Table 2-2: MAX 10 Devices Migration from ES Device DA Variant to Production Device DC or DF Variant

MAX 10 ES Device DA Variant Pin	MAX 10 Production Device DC or DF Variant Pin
ADC_VREF	VCCA
ANAIN[1..2]	GND
REFGND	GND
ADC1IN[1..16] or ADC[1..2]IN[1..8]	I/O
VCCA_ADC	VCCA
VCCINT	VCC

Document Revision History 3

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Date	Version	Changes
June 2015	2015.06.12	Updated the note in Device Errata and Device Guidelines chapters: ES devices are not intended to be used for volume production or device qualification testing.
March 2015	2015.03.06	• Added EMIF guideline: ES devices are intended to be used at nominal voltage and nominal temperature only for DDR3 external memory interface (EMIF) support. • Removed transient current guidelines. • Added Migration Guidelines.
November 2014	2014.11.11	• Added total harmonic distortion specifications for 10M08 ES devices in ADC Prescalar errata. • Added errata for timing model adjustment.
September 2014	2014.09.22	Initial release.