RealView ICE and RealView Trace

System and Interface Design Reference



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RealView ICE and RealView Trace System and Interface Design Reference

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Release Information

The following changes have been made to this book.

				Change history
Date	Issue	Confidentiality	Change	
May 2010	А	Non-confidential	First release.	

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Federal Communications Commission Notice

This device is test equipment and consequently is exempt from part 15 of the FCC Rules under section 15.103 (c).

CE Declaration of Conformity

CE

The system should be powered down when not in use.

It is recommended that ESD precautions be taken when handling RealView ICE and RealView Trace equipment.

The RealView ICE and RealView Trace modules generate, use, and can radiate radio frequency energy and may cause harmful interference to radio communications. There is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures:

- ensure attached cables do not lie across the target board
- reorient the receiving antenna
- increase the distance between the equipment and the receiver
- connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- consult the dealer or an experienced radio/TV technician for help

— Note —

It is recommended that wherever possible shielded interface cables be used.

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Chapter 1 Conventions and feedback

The following describes the typographical conventions and how to give feedback:

Typographical conventions

The following typographical conventions are used:

monospace Denotes text that can be entered at the keyboard, such as commands, f	ĩle
and program names, and source code.	

monospace Denotes a permitted abbreviation for a command or option. The underlined text can be entered instead of the full command or option name.

monospace italic

Denotes arguments to commands and functions where the argument is to be replaced by a specific value.

monospace bold

Denote	s language	keywords	when used	loutside	example code	;.
--------	------------	----------	-----------	----------	--------------	----

- *italic* Highlights important notes, introduces special terminology, denotes internal cross-references, and citations.
- **bold** Highlights interface elements, such as menu names. Also used for emphasis in descriptive lists, where appropriate, and for ARM[®] processor signal names.

Feedback on this product

If you have any comments and suggestions about this product, contact your supplier and give:

• your name and company

- the serial number of the product
- details of the release you are using
- details of the platform you are using, such as the hardware platform, operating system type and version
- a small standalone sample of code that reproduces the problem
- a clear explanation of what you expected to happen, and what actually happened
- the commands you used, including any command-line options
- sample output illustrating the problem
- the version string of the tools, including the version number and build numbers.

Feedback on content

If you have comments on content then send an e-mail to errata@arm.com. Give:

- the title
- the number, ARM DUI 0517A
- if viewing online, the topic names to which your comments apply
- if viewing a PDF version of a document, the page numbers to which your comments apply
- a concise explanation of your comments.

ARM also welcomes general suggestions for additions and improvements.

ARM periodically provides updates and corrections to its documentation on the ARM Information Center, together with knowledge articles and *Frequently Asked Questions* (FAQs).

Other information

- ARM Information Center, http://infocenter.arm.com/help/index.jsp
- ARM Technical Support Knowledge Articles, http://infocenter.arm.com/help/topic/com.arm.doc.faqs/index.html
- Keil Distributors, http://www.keil.com/distis.

Chapter 2 System Design Guidelines

The following topics provide information on developing ARM[®] architecture-based devices and *Printed Circuit Boards* (PCBs) that can be debugged using RealView[®] ICE:

- Using adaptive clocking to synchronize the JTAG port on page 2-2
- *Reset signals* on page 2-5
- *ARM reset signals* on page 2-6
- *RealView ICE reset signals* on page 2-7
- Example reset circuits on page 2-8
- ASIC guidelines on page 2-10
- ICs containing multiple devices on page 2-11
- Boundary scan test vectors on page 2-12
- PCB guidelines on page 2-13
- *PCB connections* on page 2-14
- *Target interface logic levels* on page 2-15
- JTAG signal integrity and maximum cable lengths on page 2-17.

2.1 Using adaptive clocking to synchronize the JTAG port

ARM[®] architecture-based devices using only hard macrocells, for example ARM7TDMI[®] and ARM920T, use the standard five-wire JTAG interface (**TCK**, **TMS**, **TDI**, **TDO**, and **nTRST**). Some target systems, however, require that JTAG events are synchronized to a clock in the system. To handle this case, an extra signal (**RTCK**) is included on the JTAG port. For example, this synchronization is required in:

- an ASIC with single rising-edge D-type design rules, such as one based on an ARM7TDMI-S[™] processor
- a system where scan chains external to the ARM macrocell must meet single rising-edge D-type design rules.

The adaptive clocking feature of RealView[®] ICE addresses this requirement. When adaptive clocking is enabled, RealView ICE issues a **TCK** signal and waits for the **RTCK** signal to come back. RealView ICE does not progress to the next **TCK** until **RTCK** is received.

— Note —

- If you use the adaptive clocking feature, transmission delays, gate delays, and synchronization requirements result in a lower maximum clock frequency than with non-adaptive clocking. Do not use adaptive clocking unless it is required by the hardware design.
- If, when autoconfiguring a target, the RealView ICE run control unit receives pulses on **RTCK** in response to **TCK** it assumes that adaptive clocking is required, and enables adaptive clocking in the target configuration. If the hardware does not require adaptive clocking, the target is driven slower than it could be. You can disable adaptive clocking using controls on the JTAG settings dialog box.
- If adaptive clocking is used, RealView ICE cannot detect the clock speed, and therefore cannot scale its internal timeouts. If the target clock frequency is very slow, a JTAG timeout might occur. This leaves the JTAG in an unknown state, and RealView ICE cannot operate correctly without reconnecting to the processor. JTAG timeouts are enabled by default. You can disable JTAG timeouts by deselecting the option JTAG Timeouts Enabled in the RVConfig utility.

You can use adaptive clocking as an interface to targets with slow or widely varying clock frequency, such as battery-powered equipment that varies its clock speed according to processing demand. In this system, **TCK** might be hundreds of times faster than the system clock, and the debugger loses synchronization with the target system. Adaptive clocking ensures that the JTAG port speed automatically adapts to slow system speed.

The following figure shows a circuit for a basic JTAG port synchronizer.

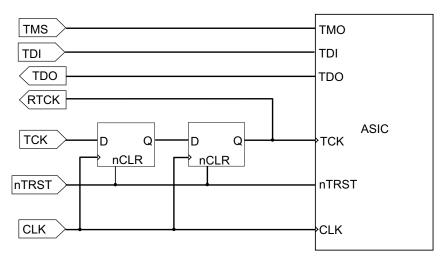


Figure 2-1 Basic JTAG port synchronizer

The following figure shows a partial timing diagram for the basic JTAG synchronizer. The delay can be reduced by clocking the flip-flops from opposite edges of the system clock, because the second flip-flop only provides better immunity to metastability problems. Even a single flip-flop synchronizer never completely misses **TCK** events, because **RTCK** is part of a feedback loop controlling **TCK**.

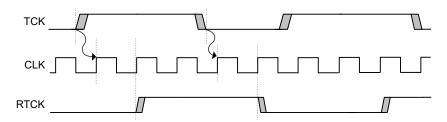


Figure 2-2 Timing diagram for the Basic JTAG synchronizer

It is common for an ASIC design flow and its design rules to impose a restriction that all flip-flops in a design are clocked by one edge of a single clock. To interface this to a JTAG port that is completely asynchronous to the system, it is necessary to convert the JTAG **TCK** events into clock enables for this single clock, and to ensure that the JTAG port cannot overrun this synchronization delay.

The following figure shows one possible implementation of this circuit.

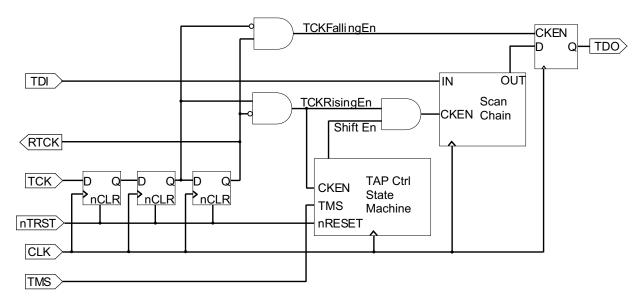


Figure 2-3 JTAG port synchronizer for single rising-edge D-type ASIC design rules

The following figure shows a corresponding partial timing diagram, and how **TCKFallingEn** and **TCKRisingEn** are each active for exactly one period of **CLK**. It also shows how these enable signals gate the **RTCK** and **TDO** signals so that they only change state at the edges of **TCK**.

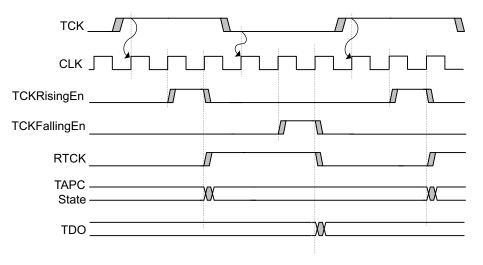


Figure 2-4 Timing diagram for the D-type JTAG synchronizer

2.1.1 See also

Concepts

- *Reset signals* on page 2-5
- ASIC guidelines on page 2-10
- *PCB guidelines* on page 2-13
- *JTAG signal integrity and maximum cable lengths* on page 2-17.

Reference

- Chapter 3 JTAG Interface Connections
- Chapter 6 Designing the Target Board for Tracing
- Chapter 7 Serial Wire Debug

2.2 Reset signals

The reset signals that are available on ARM[®] devices, and how RealView[®] ICE expects them to be wired, are described in the following topics:

- *ARM reset signals* on page 2-6
- *RealView ICE reset signals* on page 2-7
- *Example reset circuits* on page 2-8.

2.2.1 See also

Concepts

- Using adaptive clocking to synchronize the JTAG port on page 2-2
- ASIC guidelines on page 2-10
- *PCB guidelines* on page 2-13
- JTAG signal integrity and maximum cable lengths on page 2-17.

Reference

- Chapter 3 JTAG Interface Connections
- Chapter 6 Designing the Target Board for Tracing
- Chapter 7 Serial Wire Debug

2.3 ARM reset signals

All ARM[®] processors have a main processor reset that might be called **nRESET**, **BnRES**, or **HRESET**. This is asserted by one or more of these conditions:

- power on
- manual push button
- remote reset from the debugger (using RealView[®] ICE)
- watchdog circuit (if appropriate to the application).

Any ARM processor including the JTAG interface has a second reset input called **nTRST** (TAP Reset). This resets the EmbeddedICE[®] logic, the TAP controller, and the boundary scan cells. It is activated by a remote JTAG reset.

It is strongly recommended that both signals are separately available on the JTAG connector. If the **nRESET** and **nTRST** signals are linked together, resetting the system also resets the TAP controller. This means that:

- it is not possible to debug a system from reset, because any breakpoints previously set are lost
- you might have to start the debug session from the beginning, because RealView ICE does not recover when the TAP controller state is changed.

2.3.1 See also

Concepts

- RealView ICE reset signals on page 2-7
- *Example reset circuits* on page 2-8.

2.4 RealView ICE reset signals

The RealView[®] ICE run control unit has two reset signals connected to the debug target hardware:

- **nTRST** drives the JTAG **nTRST** signal on the ARM[®] processor. It is an output that is activated whenever the RealView ICE debug software has to re-initialize the debug interface in the target system.
- **nSRST** is a bidirectional signal that both drives and senses the system reset signal on the target. The output is driven LOW by the debugger to re-initialize the target system.

The target hardware must include a pull-up resistor on both reset signals. In the RealView ICE run control unit, the strong pull-up/pull-down resistance is approximately 100Ω , and the weak pull-up/pull-down resistance is approximately $4.7k\Omega$. Because you can select the drive strength for **nTRST** and **nSRST**, target assemblies with a variey of different reset configurations can be supported.

2.4.1 See also

Concepts

- *ARM reset signals* on page 2-6
- Example reset circuits on page 2-8.

Reference

Using the Debug Hardware Configuration Utilities:

Advanced configuration, ../com.arm.doc.dui0498a/CIHGABDH.html

2.5 Example reset circuits

The circuits shown in the following figures illustrate how the behavior relating to ARM[®] reset signals and RealView[®] ICE reset signals can be achieved.

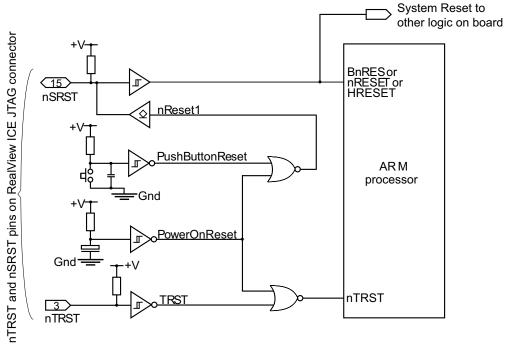


Figure 2-5 Example reset circuit logic

The symbol for nReset1 signifies a sink driver, with an open collector output.

- Note

The MAX823 used in the following figure is a typical power supply supervisor. It has a current limited **nRESET** output that can be overdriven by the RealView ICE run control unit.

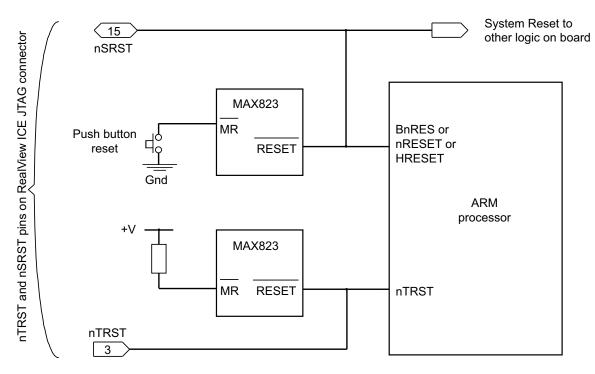


Figure 2-6 Example reset circuit using power supply monitor ICs

2.5.1 See also

Concepts

- ARM reset signals on page 2-6
- *RealView ICE reset signals* on page 2-7.

2.6 ASIC guidelines

ASIC guidelines are described in the following topics:

- *ICs containing multiple devices* on page 2-11
- *Boundary scan test vectors* on page 2-12.

2.7 ICs containing multiple devices

If your ASIC contains multiple devices that have a JTAG TAP controller, you must serially chain them so that RealView[®] ICE can communicate with all of them simultaneously. The chaining can either be within the ASIC, or externally.

—____Note _____

There is no support in RealView ICE for multiplexing TCK, TMS, TDI, TDO, and RTCK between a number of different processors.

2.7.1 TAP controllers serially chained within the ASIC

The JTAG standard originally described serially chaining multiple devices on a PCB. This concept can be extended to serially chaining multiple TAP controllers within an ASIC. This configuration does not increase the package pin count. It does increase JTAG propagation delays, but this impact can be small if you put unaddressed TAP controllers into bypass mode, as shown in the following figure:

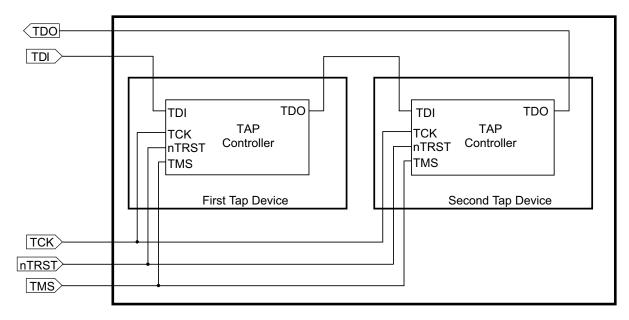


Figure 2-7 TAP Controllers serially chained within an ASIC

2.7.2 TAP controllers serially chained externally

You can use separate pins on the ASIC for each JTAG port, and serially chain them externally (for example on the PCB). This configuration can simplify device testing, and gives the greatest flexibility on the PCB. However, this is at the cost of many pins on the device package.

2.7.3 See also

Concepts

Boundary scan test vectors on page 2-12.

Other information

CoreSight Technology System Design Guide, http://infocenter.arm.com/help/topic/com.arm.doc.dgi0012-

2.8 Boundary scan test vectors

If you use the JTAG boundary scan test methodology to apply production test vectors, you might want to have independent external access to each TAP controller. This avoids the requirement to merge test vectors for more than one block in the device. One solution to this is to adopt a hybrid, using a pin on the package that switches elements of the device into a test mode. This can be used to break the internal daisy chaining of **TDO** and **TDI** signals, and to multiplex out independent JTAG ports on pins that are used for another purpose during normal operation.

2.8.1 See also

Concepts

ICs containing multiple devices on page 2-11.

2.9 PCB guidelines

PCB guidelines on the physical and electrical connections present on the target board are described in the following topics:

- *PCB connections* on page 2-14
 - Target interface logic levels on page 2-15.

You must consider the following:

- JTAG interface connector pinouts
- the properties of a board that can be connected to RealView Trace
- Serial Wire Debug (SWD) connections.

2.9.1 See also

Concepts

•

- ASIC guidelines on page 2-10
- JTAG signal integrity and maximum cable lengths on page 2-17.

Reference

- Chapter 3 JTAG Interface Connections
- Chapter 6 Designing the Target Board for Tracing
- Chapter 7 Serial Wire Debug.

2.10 PCB connections

It is recommended that you place the 20-way JTAG header as closely as possible to the target device, because this minimizes any possible signal degradation caused by long PCB tracks. The header must be a 0.1 inch pitch standard box header.

The following figure shows the layout of possible PCB connections:

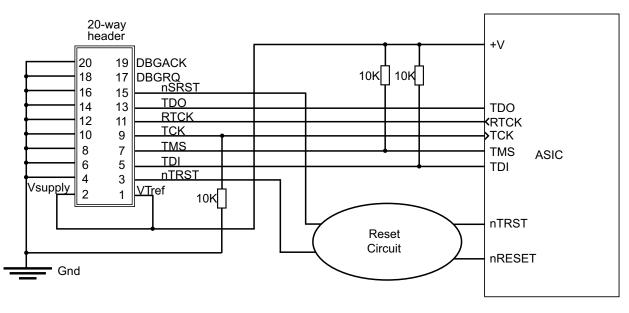


Figure 2-8 Typical PCB connections

_____ Note _____

- The signals TMS and TDI must be pulled up on the PCB, as shown.
- TCK must be pulled down on the PCB, as shown.
- **DBGRQ** and **DBGACK** are not used by the ARM[®] tools, but are used by some third party tools. If your tools do not use **DBGRQ** and **DBGACK**, and your device has a **DBGRQ** input, this must be pulled down on the PCB.
- **RTCK** is used by -S processor variants, such as the ARM966E-S processor. If your device does not use **RTCK**, then **RTCK** must be pulled down on the PCB.

2.10.1 See also

Concepts

Target interface logic levels on page 2-15.

2.11 Target interface logic levels

RealView[®] ICE is designed to interface with a wide range of target system logic levels. It does this by adapting its output drive and input threshold to a reference voltage supplied by the target system.

VTref (pin 1 on the JTAG header connector) feeds the reference voltage to the RealView ICE run control unit. This voltage, clipped at approximately 3.2V, is used as the output high voltage (Voh) for logic 1s (ones) on TCK, TDI, and TMS. 0V is used as the output low voltage for logic 0s (zeroes). The input logic threshold voltage (Vi(th)) for the TDO, RTCK, and nSRST inputs is 50% of the Voh level, and so is clipped to approximately 1.6V. The relationships of Voh and Vi(th) to VTref are shown in the following figure:

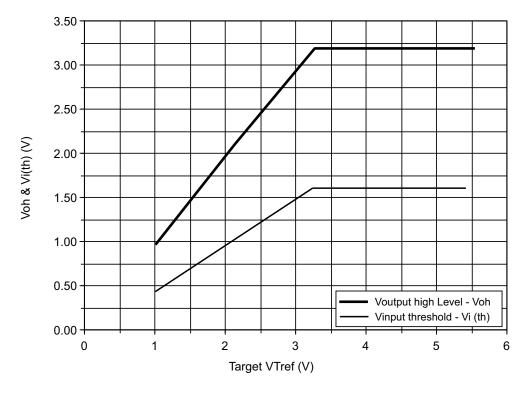


Figure 2-9 Target interface logic levels

RealView ICE can adapt interface levels down to **VTref** less than 1V. If, however, **VTref** becomes less than approximately 0.55V, RealView ICE interprets this condition as Target Not Present, and the software reports this as an error condition.

The **nTRST** output from RealView ICE is effectively driven as an active low signal, so it is actively pulled to 0V but relies on a $4.7k\Omega$ pull-up resistor to end the reset state. This is because it is common to wire-OR this signal with another source of **nTRST**, such as power-on reset in the target system.

The **nSRST** output from RealView ICE is a similarly-driven active low signal, and must be pulled-up with a resistor in the target system. Because this signal is also an input to the RealView ICE run control unit, there is a $4.7k\Omega$ internal pull-up resistor. This is to avoid spurious lows on the input when **nSRST** is not connected to the target system.

The input and output characteristics of the RealView ICE run control unit are compatible with logic levels from TTL-compatible, or CMOS logic in target systems. For information when assessing compatibility with other logic systems:

- the output impedance on the *Low Voltage Differential Signaling* (LVDS) probe of the TCK, TMS, and TDI signals is approximately 47Ω
- the output impedance of all other signals is approximately 100Ω .

2.11.1 See also

Concepts

- *RealView ICE reset signals* on page 2-7
- *PCB connections* on page 2-14.

2.12 JTAG signal integrity and maximum cable lengths

For JTAG-based debugging, you must have a very reliable connection between RealView[®] ICE and the target, because there is no way to detect or correct errors. For this reason it is important to guarantee good signal integrity.

One factor that can limit the maximum cable length is propagation delays. Normally the RealView ICE run control unit samples data returning from the target using the same clock as for sending data, **TCK**. If the propagation delay gets too long then the RealView ICE run control unit samples the signal at the wrong time. This can be resolved by using *adaptive clocking*. In this mode the target returns a clock, **RTCK**, and RealView ICE does not sample data on **TDO**, or send more data on **TDI**, until clocked by this signal.

In an ASIC or ASSP (for example, in ARM[®] processor based microcontrollers) the **TDO** and **RTCK** signals are not typically implemented with a stronger driver than other signals on the device. The strength of these drivers varies from device to device. An example specification is to sink or source 4mA. Many designs connect these pins on the device directly to the corresponding pins on the RealView ICE connector.

Over very short lengths of cable, such as the one supplied with RealView ICE, this type of weak driver is adequate. However, if longer cables are used then the cable becomes harder to drive as the capacitive load increases. When using longer cables it becomes essential to consider the cable as a transmission line and to provide appropriate impedance matching, otherwise reflections occur.

RealView ICE has much stronger drivers and they are connected through 100Ω series resistors to impedance match with the JTAG cable. This is very much better than the typical circuit used at the target end.

With the typical situation at the target end (weak drivers, no impedance matching resistors) you can only expect reliable operation over short cables (approximately 30cm). If operation over longer cables is required:

- For very long cables, a solution is to buffer the JTAG signals through differential drivers, such as the *Low Voltage Differential Signaling* (LVDS) cable and probe supplied with RealView ICE. Reliable operation is possible over tens of meters using this technique.
- For intermediate lengths of cables, you can instead improve the circuitry used at the target end. The recommended solution is to add an external buffer with good current drive and a 100 Ω series resistor for the **TDO** (and **RTCK** if used) signals on your target hardware. Using this technique you can debug over cable lengths up to several meters. Depending on cable length and propagation delays through your buffers and cables, it might still be necessary to use adaptive clocking.

If you are not already using adaptive clocking in your design, you can generate **RTCK** at the target end by using the **TCK** signal fed through the same buffer and impedance matching circuit as used for **TDO**.

Reducing the clock speed used by RealView ICE avoids some, but not all, of the problems associated with long cables. If reducing the speed of downloading code and reading memory in the debugger is not a significant problem, try experimenting with lowering this clock speed.

2.12.1 See also

Concepts

- ASIC guidelines on page 2-10
- *PCB guidelines* on page 2-13.

Reference

- Chapter 3 JTAG Interface Connections
- Chapter 6 Designing the Target Board for Tracing
- Chapter 7 Serial Wire Debug.

Chapter 3 JTAG Interface Connections

The following topics provide descriptions of the interface connections on the RealView® ICE unit:

- *JTAG interface pinouts* on page 3-2
- JTAG interface signals on page 3-3
- JTAG port timing characteristics on page 3-6.

3.1 JTAG interface pinouts

The RealView[®] ICE run control unit is supplied with a short ribbon cable, and a longer ribbon cable and *Low Voltage Differential Signaling* (LVDS) probe. These both terminate in a 20-way 2.54mm pitch *Insulation Displacement Connector* (IDC) connector. You can use either cable to mate with a keyed box header on the target. The pinout is shown in the following figure:

VTref	1	•	• 2		Vsupply
nTRST	3	•	• 4		GND
TDI	5	•	• 6		GND
TMS	7	•	• 8		GND
тск	9	•	• 10		GND
RTCK	11	•	• 12		GND
tdo l	1 ¹³	•	• 14		GND
nSRS T	15	•	• 16		GND
DBGRQ	17	•	• 18		GND
DBGACK	19	•	• 20		GND
				-	

Figure 3-1 JTAG interface pinout

_____Note _____

All GND pins must be connected to 0V on the target hardware.

3.1.1 See also

Concepts

- JTAG interface signals on page 3-3
- JTAG port timing characteristics on page 3-6.

Reference

• Chapter 4 User I/O Connections.

3.2 JTAG interface signals

The following table describes the signals on the JTAG interfaces:

Table 3-1 JTAG signals

Signal	I/O	Description	
DBGACK	-	This pin is connected in the RealView [®] ICE run control unit, but is not supported in the current release of the software. It is reserved for compatibility with other equipment to be used as a debug acknowledge signal from the target system. It is recommended that this signal is pulled LOW on the target.	
DBGRQ	-	This pin is connected in the RealView ICE run control unit, but is not supported in the current release of the software. It is reserved for compatibility with other equipment to be used as a debug request signal to the target system. The RealView ICE software maintains this signal as LOW. When applicable, RealView ICE uses the scan chain 2 of the processor to put the processor in debug state. It is recommended that this signal is pulled LOW on the target.	
GND	-	Ground.	
nSRST	Input/output	Active Low output from RealView ICE to the target system reset, with a $4.7k\Omega$ pull-up resistor for de-asserted state. This is also an input to RealView ICE so that a reset initiated on the target can be reported to the debugger. This pin must be pulled HIGH on the target to avoid unintentional resets when there is no connection.	
nTRST	Output	Active Low output from RealView ICE to the Reset signal on the target JTAG port, driven to the VTref voltage for de-asserted state. This pin must be pulled HIGH on the target to avoid unintentional resets when there is no connection.	
RTCK	Input	Return Test Clock signal from the target JTAG port to RealView ICE. Some targets must synchronize the JTAG inputs to internal clocks. To assist in meeting this requirement, you can use a returned, and retimed, TCK to dynamically control the TCK rate. RealView ICE provides Adaptive Clock Timing, that waits for TCK changes to be echoed correctly before making more changes. Targets that do not have to process TCK can ground this pin. RTCK is not supported in <i>Serial Wire Debug</i> (SWD) mode.	
ТСК	Output	Test Clock signal from RealView ICE to the target JTAG port. It is recommended that this pin is pulled LOW on the target.	
TDI	Output	Test Data In signal from RealView ICE to the target JTAG port. It is recommended that this pin is pulled HIGH on the target.	
TDO	Input	Test Data Out from the target JTAG port to RealView ICE. It is recommended that this pin is pulled HIGH on the target.	

Table 3-1 JTAG signals (continued)

Signal	I/O	Description
TMS	Output	Test Mode signal from RealView ICE to the target JTAG port. This pin must be pulled HIGH on the target so that the effect of any spurious TCK s when there is no connection is benign.
Vsupply	Input	This pin is not connected in the RealView ICE unit. It is reserved for compatibility with other equipment to be used as a power feed from the target system.
VTref	Input	This is the target reference voltage. It indicates that the target has power, and It must be at least 0.628V. VTref is normally fed from V_{dd} on the target hardware and might have a series resistor (though this is not recommended). There is a 10k Ω pull-down resistor on VTref in RealView ICE.

3.2.1 JTAG interface signal details

VTref is used to create the logic-level reference for the input comparators on TDO, RTCK and nSRST. RealView ICE clips the logic-level reference to 3.3V. RealView ICE inputs (TDO, RTCK and nSRST) are taken to high-impedance inputs of comparators. Each input is read as a logic 1 when it exceeds half the voltage reference.

VTref also controls the output logic levels to the target. RealView ICE uses analog switches to drive the output signals. The output is connected to ground for a logic 0 and to the JTAG interface voltage for a logic 1.

TDI, **TMS** and **TCK** have 47Ω series resistors on the *Low Voltage Differential Signaling* (LVDS) probe. All other outputs from the LVDS probe and the RealView ICE 20-way connector have 100 Ω series resistors.

nSRST and **nTRST** are both active low signals. When asserted, both these signals are connected to ground for a logic 0. When de-asserted, nSRST uses a $4.7k\Omega$ pull-up for a logic 1, whereas nTRST is driven to the VTref voltage for de-asserted state.

You must ensure that your board has appropriate pull-up and pull-down resistors on the JTAG signals:

- TMS, TDI, TDO, nSRST and nTRST must have pull-ups.
- TCK must have a pull-down to enable hot swap and post-mortem debugging
- **RTCK** must have a pull-down to fix a stable value on that signal when debugging a non-synthesizable processor.
- **DBGRQ** must have a pull-down. This ensures that the processor does not enter debug state in an uncontrolled way.
- **DBGACK** must have a pull-down, so the default value that the debugger sees is processor not in debug state.

The recommended value for pull-ups and pull-downs is $10k\Omega$, although the optimum value depends on the signal load. For example, pull-downs must be about $1k\Omega$ when working with TTL logic.

3.2.2 See also

Concepts

JTAG interface pinouts on page 3-2

• JTAG port timing characteristics on page 3-6.

Reference

• Chapter 4 User I/O Connections.

3.3 JTAG port timing characteristics

You must consider the timing characteristics of a RealView[®] ICE unit if you design a target device or board and want to be able to connect RealView ICE at a particular **TCK** frequency. The characteristics relate to the RealView ICE hardware. You must consider them in parallel with the characteristics of your target.

The following figure shows the JTAG port timing and parameters:

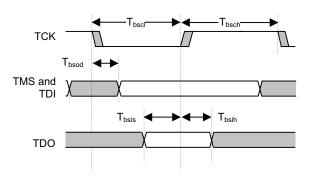


Figure 3-2 JTAG port timing diagram

In a JTAG device that fully complies to IEEE1149.1-2001, **TDI** and **TMS** are sampled on the rising edge of **TCK**, and **TDO** changes on the falling edge of **TCK**. To take advantage of these properties, RealView ICE samples **TDO** on the rising edge of **TCK** and changes its **TDI** and **TMS** signals on the falling edge of **TCK**. This means that with a fully compliant target, issues with minimum setup and hold times can always be resolved by decreasing the **TCK** frequency, because this increases the separation between signals changing and being sampled.

_____Note ____

There are no separate timing requirements for adaptive clocking mode, because the minimum T_{bsch} and T_{bscl} times are identical and are the same as for non-adaptive clocking. T_{bsis} and T_{bsih} are relative to RTCK rising, and not TCK rising, as RTCK is used to sample TDO in adaptive clocking mode.

The only real timing difference is that in adaptive mode, RealView ICE samples **TDO** on the rising edge of **RTCK** and not **TCK**, so **TDO** timing is relative to **RTCK**.

The following table shows the timing requirements for the JTAG A port, measured open circuit (no target connection, except for 3.3V reference on **VTref**) with the supplied JTAG cable connected:

	Table		New IOE TIAG A timing requirements
Parameter	Min	Мах	Description
T _{bscl}	50ns	500µs	TCK LOW period
T _{bsch}	50ns	500µs	TCK HIGH period
T _{bsod}	-	6.0ns	TDI and TMS valid from TCK (falling)
T _{bsis}	15.0ns	-	TDO setup to TCK (rising)
T _{bsih}	6.0ns	-	TDO hold from TCK (rising)

The following table shows the timing requirements for the JTAG B port, measured open circuit (no target connection, except for 3.3V reference on **VTref**) with no cable connected:

Parameter	Min	Мах	Description
T _{bsc1}	10ns	500µs	TCK LOW period
T _{bsch}	10ns	500µs	TCK HIGH period
T _{bsod}	-	3.2ns	TDI and TMS valid from TCK (falling)
T _{bsis}	6.2ns	-	TDO setup to TCK (rising)
T _{bsih}	4.5ns	-	TDO hold from TCK (rising)

Table 3-3 RealView ICE JTAG B timing requirements

— Note —

- The RealView ICE software enables you to change the **TCK** frequency. The **TCK** LOW:HIGH mark-space ratio is always 50:50. The other parameters must be considered with the specific values of T_{bscl} and T_{bsch} that you have chosen. The default values for an autoconfigured single-TAP system are, nominally, T_{bscl}=50ns and T_{bsch}=50ns.
- T_{bsod} is the maximum delay between the falling edge of **TCK** and valid levels on the **TDI** and **TMS** RealView ICE output signals. The target samples these signals on the following rising edge of **TCK** and so the minimum setup time for the target, relative to the rising edge of **TCK**, is T_{bsc1}-T_{bsod}.
- T_{bsis} is the minimum setup time for the **TDO** input signal, relative to the rising edge of **TCK** when RealView ICE samples this signal. The target changes its **TDO** value on the previous falling edge of **TCK** and so the maximum time for the target **TDO** level to become valid, relative to the falling edge of **TCK**, is T_{bscl}-T_{bsis}.

3.3.1 See also

Concepts

- JTAG interface pinouts on page 3-2
- *JTAG interface signals* on page 3-3.

Reference

Chapter 4 User I/O Connections.

Chapter 4 User I/O Connections

The following topic describes the additional input and output connections provided in RealView[®] ICE, and consists of:

• The RealView ICE User I/O connector on page 4-2.

4.1 The RealView ICE User I/O connector

The User *Input/Output* (I/O) connector is situated on an end panel of the RealView[®] ICE unit. The connector is a 10-way 2.54mm pitch *Insulation Displacement Connector* (IDC) header that mates with IDC sockets mounted on a ribbon cable, as shown in the following figure.

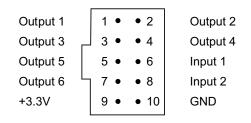


Figure 4-1 User I/O pin connections

— Warning ——

You must establish a common ground between the RealView ICE unit and the target hardware before you connect any of the User I/O signals.

The following table shows the User I/O pin connections.

			-
Pin	Signal	I/O	Description
Pin 1	Output 1	Output	This is a user output bit. It operates at a 3.3V swing, with a 100Ω series resistance.
Pin 2	Output 2	Output	This is a user output bit. It operates at a 3.3V swing, with a 100Ω series resistance.
Pin 3	Output 3	Output	This is a user output bit. It operates at a 3.3V swing, with a 100Ω series resistance.
Pin 4	Output 4	Output	This is a user output bit. It operates at a 3.3V swing, with a 100Ω series resistance.
Pin 5	Output 5	Output	This is a user output bit. It operates at a 3.3V swing, with a 100Ω series resistance.
Pin 6	Input 1	Input	This is a user input bit. It has a $10k\Omega$ weak pull-up to the unit internal +3.3V supply, and requires a $V_{ih(min)}$ of 2.0V and a $V_{il(max)}$ of 0.8V. It can safely be driven by 5V logic levels, and has <i>Electro Static Discharge</i> (ESD) protection greater than the 2kV human body model. This pin is not currently supported.
Pin 7	Output 6	Output	This is a copy of the trigger output on the end panel of the RealView ICE unit. It operates at a 3.3V swing, with a 100Ω series resistance.

Table 4-1 User I/O pin connections

Table 4-1 User I/O pin connections (continued)

Pin	Signal	I/O	Description
Pin 8	Input 2	Input	This is a copy of the trigger input on the end panel of the RealView ICE unit. It has a $10k\Omega$ weak pull-up to the unit internal +3.3V supply, and requires a $V_{ih(min)}$ of 2.0V and a $V_{il(max)}$ of 0.8V. It can safely be driven by 5V logic levels, and has ESD protection greater than the 2kV human body model. This pin is not currently supported.
Pin 9	+3.3V	Output	This is intended for powering external signal conditioning circuitry, to a maximum current of 100mA. Incorrect use of this output might cause the RealView ICE unit to enter current limit.
Pin 10	GND	-	-

_____Note _____

Input is not currently supported on the User I/O pin connections.

4.1.1 See also

Reference

Setting up the Hardware:

• The RealView ICE run control unit on page 2-10.

Chapter 5 RealView Trace and RealView Trace 2 signals

The following topic describes the RealView® Trace and RealView Trace 2 signals:

• *Trace signals* on page 5-2.

5.1 Trace signals

Data transfer is synchronized by the **TRACECLK** signal. See the following:

- Signal levels
- Clock frequency
- Switching thresholds
- Hot-plugging.

5.1.1 Signal levels

The maximum capacitance presented by trace at the trace port connector, including the connector and interfacing logic, is less than 6pF. The trace port lines have a matched impedance of 50Ω .

The RealView[®] Trace unit operates with a target board that has a supply voltage range of 1.0V-5.0V.

5.1.2 Clock frequency

For capturing trace port signals synchronous to **TRACECLK**, RealView Trace supports a **TRACECLK** frequency of up to 250MHz, and RealView Trace 2 supports up to 480MHz. These frequencies must be halved if capturing trace using half-rate clocking (DDR) mode. The following figure and table describe the timing for **TRACECLK** in SDR clocking mode.

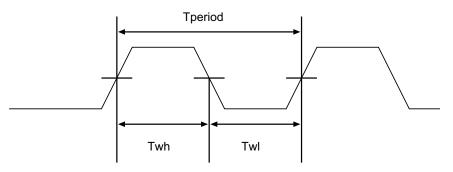


Figure 5-1 Clock waveforms

Table 5-1 TRACECLK frequencies

Parameter	RVT1	RVT2	Description
Tperiod (min)	4.0ns	2.08ns	Clock period
Twh (min)	1.5ns	1.0ns	High pulse width
Twl (min)	1.5ns	1.0ns	Low pulse width

5.1.3 Switching thresholds

The RealView Trace probe detects the target signaling reference voltage (VTref) and automatically adjusts its switching thresholds to VTref/2. For example, on a 3.3 volt target system, the switching thresholds are set to 1.65 volts.

5.1.4 Hot-plugging

RealView Trace is not damaged if it is powered up when plugged into an unpowered target or if an unpowered RealView Trace unit is plugged into a powered target.

If both the RealView Trace unit and the target are powered, no damage occurs to the RealView Trace unit, but there might be damage to a (third-party) target system.

5.1.5 See also

References

•

ETMv1 and ETMv3 architecture pinouts, http://infocenter.arm.com/help/topic/com.arm.doc.ihi0014-

Chapter 6 Designing the Target Board for Tracing

The following topics describe the properties of a target board that can be connected to RealView[®] Trace:

- Overview of high-speed design on page 6-2
- Signal termination on page 6-3
- *Termination example* on page 6-4
- Series termination on page 6-5
- *Rules for series terminators* on page 6-6
- PCB track impedance on page 6-7
- Probes, dimensions and keep out areas on page 6-8
- Dual-Mictor trace probe for RealView Trace 2 on page 6-9
- Dual-Mictor trace probe characteristics on page 6-11
- Signal requirements on page 6-12
- *Probe modeling* on page 6-14.

6.1 Overview of high-speed design

Failure to observe high-speed design rules when designing a target system containing an ARM[®] *Embedded Trace Macrocell* (ETM) trace port can result in incorrect data being captured by RealView[®] Trace. You must give serious consideration to high-speed signals when designing the target system.

The signals coming from an ARM ETM trace port can have very fast rise and fall times, even at relatively low frequencies. For example, a signal with a rise time of 1ns has an effective knee frequency of 500MHz and a signal with a rise time of 500ps has an effective knee frequency of 1GHz ($f_{knee} = 0.5/Tr$).

```
—— Note ———
```

These principles apply to all of the trace port signals, but special care must taken with **TRACECLK**.

You must make the following considerations for high-speed design:

Avoid stubs

Stubs are short pieces of track that tee off from the main track carrying the signal to, for example, a test point or a connection to an intermediate device. Stubs cause impedance discontinuities that affect signal quality and must be avoided.

Special care must therefore be taken when ETM signals are multiplexed with other pin functions and where the PCB is designed to support both functions with differing tracking requirements.

Minimize signal skew (balancing PCB track lengths)

You must attempt to match the lengths of the PCB tracks carrying the trace port signals from the ASIC to the Mictor connector to within approximately 0.5 inches (12.5mm) of each other. Any greater differences directly impact the setup and hold time requirements.

Minimize crosstalk

Normal high-speed design rules must be observed. For example, do not run dynamic signals parallel to each other for any significant distance, keep them spaced well apart, and use a ground plane and so forth. Particular attention must be paid to the **TRACECLK** signal. If in any doubt, place grounds or static signals between the **TRACECLK** and any other dynamic signals.

Use impedance matching and termination

Termination is almost certainly necessary, but there are some circumstances where it is not required. The decision is related to track length between the ASIC and the Mictor connector.

6.1.1 See also

- Signal termination on page 6-3
- Probes, dimensions and keep out areas on page 6-8
- Signal requirements on page 6-12
- *Probe modeling* on page 6-14.

6.2 Signal termination

To calculate the maximum track length that can be used without termination, you must know the following about your ASIC and PCB:

- the rise time (Tr) of the signals coming off the ASIC
- the impedance of the output drivers on the ASIC for the ETM signals
- the propagation delay per inch of PCB track (Tpdt).

6.2.1 See also

- *Termination example* on page 6-4
- Series termination on page 6-5
- *Rules for series terminators* on page 6-6
- *PCB track impedance* on page 6-7.

6.3 **Termination example**

The maximum track length without termination is given by:

 $Length_{(inches)} < \frac{Tr_{(ps)}}{5 Tpdt_{(ps)}}$

That is, the signal propagation delay from the ASIC to the Mictor connector must be less than one fifth of the signal rise time. This calculation allows for the delay of the Mictor connector and the delay of the track from the Mictor to the input buffers on the probe.

For a case where the signal rise time (Tr) is 1ns (1000ps) and the propagation delay of the trace (Tpdt) is 160ps per inch (typical for a PCB made with FR4 laminate), L must be less than 1000/(5 * 160). That is, L must be less than 1.25 inches. If the PCB trace length from the ASIC to the Mictor connector is greater than 1.25 inches, you must use termination.

6.3.1 See also

Concepts

•

- Series termination on page 6-5
- Rules for series terminators on page 6-6
- PCB track impedance on page 6-7.

6.4 Series termination

Series (or source) termination is a technique employed in point-to-point signaling to ensure that no excessive overshoot or ringing occurs. This is achieved by reducing the source voltage by approximately 50% close to the driver. When the signal reaches the end of the transmission line, the high impedance of the receiver causes a reflection which approximately doubles the signal back to its original amplitude. When the reflection returns to the series terminating resistor, the potential across the resistor drops to zero which prevents any more current from entering the transmission line. From the perspective of the receiver, this gives a perfect 100% logic transition without any overshoot or ringing.

It is recommended that all outputs from the target system be simulated to ensure that a reliable signal is delivered to the RealView[®] ICE probe. Some overshoot/undershoot is acceptable but it is recommended to keep this below ~0.5V. Beyond this point, the clamping diodes at the receivers will start to cause high transient currents which in turn cause increased crosstalk, radio emissions and target power usage.

The target signal impedance for use with RealView ICE is 50Ω .

The following table lists some typical series terminating resistor values for instances when the outputs cannot be simulated.

Driver strength	Typical series terminator	
32mA	39Ω	Best signal integrity, highest speed
24mA	33Ω	-
16mA	27Ω	-
12mA	22Ω	-
8mA	15Ω	-
6mA	10Ω	Worst signal integrity, lowest speed

Table 6-1 Typical series terminating resistor values

Some types of IC use "impedance matched" outputs to improve their signal integrity. This is usually achieved by using weaker drive transistors to slow down the edge transitions. This has the side effect of limiting the data throughput of the driver.

To achieve the highest data rates with the best signal integrity, it is recommended to use a strong and fast driver and appropriate series terminating resistor.

If it is determined that series terminating resistors are not required, it is recommended that 0Ω links be placed close to the driver as a fall-back option.

When series terminating multiple signals, it is common to use small quad resistor packages. This saves board space and reduces parasitic effects without much risk of placement or tombstoning issues during production.

6.4.1 See also

- Termination example on page 6-4
- *Rules for series terminators* on page 6-6
- *PCB track impedance* on page 6-7.

6.5 Rules for series terminators

Series (source) termination is the most commonly used method. The basic rules are:

- The series resistor must be placed as close as possible to the ASIC pin (less than 0.5 inches)
- The value of the resistor must equal the impedance of the track minus the output impedance of the output driver. So for example, a 50Ω PCB track driven by an output with a 17Ω impedance, requires a resistor value of 33Ω .

_____Note _____

It is recommended that the overall source impedance be as close as possible to 50Ω .

• A source terminated signal is only valid at the end of the signal path. At any point between the source and the end of the track, the signal appears distorted because of reflections. Any device connected between the source and the end of the signal path therefore sees the distorted signal and might not operate correctly. Care must be taken not to connect devices in this way, unless the distortion does not affect device operation.

6.5.1 See also

- *Termination example* on page 6-4
- Series termination on page 6-5
- *PCB track impedance* on page 6-7.

6.6 PCB track impedance

Use the following formula only for microstrips (track on outer layer over a ground plane):

Impedance =
$$\frac{87}{\sqrt{(E_r + 1.41)}}$$
 In $\left[\frac{5.98h}{(0.81w + t)}\right] \Omega$

where:

hHeight above ground plane (inches)wTrace width (inches), and 0.1 < w/h < 2tTrace thickness (inches) E_r Relative permittivity of processor/prepreg, and $1 < E_r < 15$

The dimensions h, w, and t are shown in the following figure.

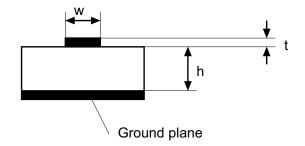


Figure 6-1 Track impedance

As an example, the following track (in microstrip form) has an impedance of 51.96Ω:

- h 0.005 inch height above ground
- w 0.007 inch width track
- t 0.0014 inch thickness (1 oz. finished weight)
- E_r 4.5 (FR4 laminate)

— Note —

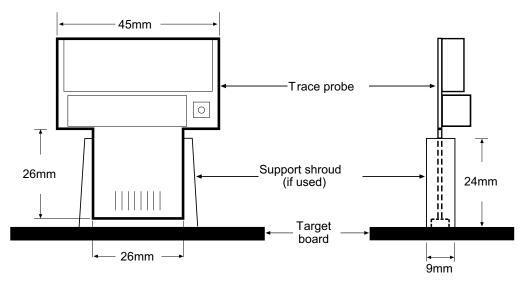
As the track width increases, the impedance decreases.

6.6.1 See also

- *Termination example* on page 6-4
- Series termination on page 6-5
- *Rules for series terminators* on page 6-6.

6.7 Probes, dimensions and keep out areas

The following figure shows a single-connector Trace probe in RealView[®] Trace attached to a target board:



```
Figure 6-2 Probe dimensions
```

——Caution ———

The Mictor connector is not robust. It is recommended that the plastic shroud is fitted around the target connector. This part is not supplied as standard with RealView Trace.

The Mictor connector support shroud is available from Agilent as Part Number E5346 - 44701.

6.7.1 See also

- Overview of high-speed design on page 6-2
- Signal termination on page 6-3
- Dual-Mictor trace probe for RealView Trace 2 on page 6-9
- Dual-Mictor trace probe characteristics on page 6-11
- Signal requirements on page 6-12
- Probe modeling on page 6-14.

6.8 Dual-Mictor trace probe for RealView Trace 2

A 32-bit, dual-Mictor trace probe is available for use with RealView[®] Trace 2 units. This probe is connected to the 40- and 60-way trace probe connectors on the RVT 2 unit using a split-ribbon cable. The following figure shows the dual-Mictor trace probe.

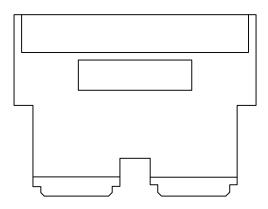


Figure 6-3 32-bit dual-Mictor trace probe

A typical arrangement using the dual-Mictor trace probe is shown in the following figure.

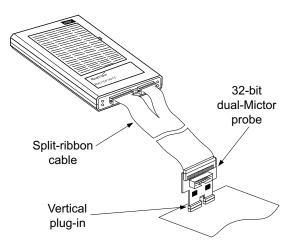


Figure 6-4 RealView Trace 2 unit connections

It is possible to use extender cables for connecting the dual-Mictor probe to the trace connector on the target board. See the following figure.

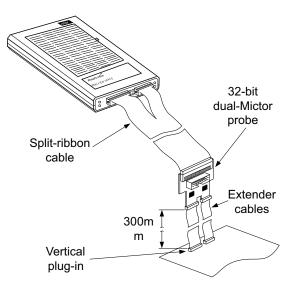


Figure 6-5 Dual-Mictor probe with extender cables

— Note ——— If extender cables are used, for optimum results the maximum length of these must not exceed 300mm.

——— Note ————

It is not recommended that you use the extender cables for targets with a trace clock over 300MHz.

6.8.1 See also

Concepts

- Probes, dimensions and keep out areas on page 6-8 •
- Dual-Mictor trace probe characteristics on page 6-11 •
- Probe modeling on page 6-14. ٠

6.9 Dual-Mictor trace probe characteristics

The spacing between the dual connectors is shown in the following figure.

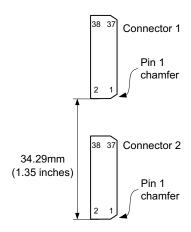


Figure 6-6 Dual-Mictor pitch dimensions

The pitch tolerance is 0.1mm.

— Note ——

If connection is to be made to a target that does not fulfil these position requirements, the Dual Mictor Extender Cable Kit (Part Number RT200-CB-00032), comprising two Mictor extender cables, can be used to connect the probe to the target. For more information on the Cable Kit, contact your supplier.

Single-length extender cables have a rating of 400Mbps.

6.9.1 See also

- Probes, dimensions and keep out areas on page 6-8
- Dual-Mictor trace probe for RealView Trace 2 on page 6-9
- *Probe modeling* on page 6-14.

6.10 Signal requirements

The data setup and hold requirements are described in the following:

- Data setup and hold
- Switching Thresholds
 - Hot-plugging.

6.10.1 Data setup and hold

The following figure and table show the setup and hold timing of the trace signals with respect to **TRACECLK**.

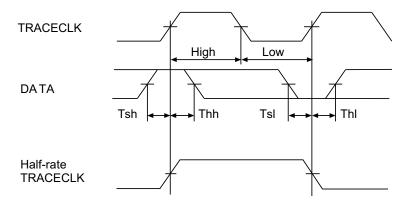


Figure 6-7 Data waveforms

Table 6-2 Data setup and hold

Parameter	RVT1	RVT2	Description
Tsh (min)	2.0ns	1.0ns	Data setup high
Thh (min)	1.0ns	1.0ns	Data hold high
Tsl (min)	2.0ns	1.0ns	Data setup low
Thl (min)	1.0ns	1.0ns	Data hold low

— Note ———

RealView[®] Trace supports half-rate clocking mode. Data is output on each edge of the **TRACECLK** signal and **TRACECLK (max)** <= 125MHz for RVT1, and <=240MHz for RVT2.

6.10.2 Switching Thresholds

The RealView Trace probe senses the target signaling reference voltage (VTref) and automatically adjusts its switching thresholds to VTref/2. For example, on a 3.3 volt target system, the switching thresholds are set to 1.65 volts.

6.10.3 Hot-plugging

If both RealView Trace and the target are powered, plugging or unplugging the trace cable does not damage or crash the RealView Trace system. It is not possible, however, to guarantee similar immunity to any third party target system. You must, therefore, take precautions such as pulling inputs and driving or making high Z outputs when **Vsupply** is not present.

6.10.4 See also

Concepts

•

- Overview of high-speed design on page 6-2
- Signal termination on page 6-3
- Probes, dimensions and keep out areas on page 6-8
- *Probe modeling* on page 6-14.

6.11 Probe modeling

For **TRACECLK** frequencies above 100MHz, it is recommended that modeling is used. The characteristics for the RealView[®] Trace probe are:

The Mictor connector single line model can be downloaded directly from the AMP web site. The closest available model is entitled *MICTOR*, .025" *PITCH*, 2 *ROW*, *VERTICAL PLUG TO VERTICAL RECEPTACLE*, 0.260" [6.6mm] *HEIGHT*.

The connector assembly (plug and receptacle together) can be viewed as a transmission line with an impedance of 45Ω and a propagation delay of 39ps. For more accurate modeling, multi-line models can be requested from AMP.

- All traces are microstrips (on outer layers over ground planes).
- All traces are designed to a target impedance of $50\Omega \pm 2\Omega$.
- Trace lengths from Mictor to input buffers are 0.329 inches maximum and 0.193 inches minimum.
- Average trace separation is 0.010 inches.
- Er = 4.5.
- The probe input buffers are a mixture of Fairchild FIN1104MTD and FIN1108MTD devices (4 channel & 8 channel devices respectively).

The datasheets, ibis and hspice models for these devices are available on the Fairchild web site.

6.11.1 See also

Concepts

- Overview of high-speed design on page 6-2
- Signal termination on page 6-3
- *Probes, dimensions and keep out areas* on page 6-8
- Signal requirements on page 6-12.

Other information

- AMP web site , http://www.amp.com
- Models at AMP, http://www.amp.com/simulation/scripts/models.asp
- Fairchild web site , http://www.fairchildsemi.com

Chapter 7 Serial Wire Debug

The *Serial Wire Debug* (SWD) connection to the *Debug Access Port* (DAP), and the functionality available for use with the *Low Voltage Differential Signaling* (LVDS) probe, are described in the following:

- *Target interface* on page 7-2
- *SWD timing requirements* on page 7-3.

7.1 Target interface

The functionality available for use with the *Low Voltage Differential Signaling* (LVDS) probe supports a *Serial Wire Debug* (SWD) connection to the *Debug Access Port* (DAP). SWD is an alternative protocol to JTAG for connecting to CoreSight processors, and has the advantage of requiring fewer pins than previous probes. It also supports higher data rates.

The following table shows the SWD pinout for the connector alongside the JTAG pinout.

Table	7-1	SWD	interface	pinout
TUNIO		0115		pinout

Pin	Signal		Pin	Circul
	JTAG	Serial Wire	PIN	Signal
1	VTref	VTref	2	NC
3	nTRST	NC	4	GND
5	TDI	NC	6	GND
7	TMS	SWDIO	8	GND
9	ТСК	SWDCLK	10	GND
11	RTCK	NC	12	GND
13	TDO	SWO	14	GND
15	nSRST	nSRST	16	GND
17	DBGRQ	DBGRQ	18	GND
19	DBGACK	DBGACK	20	GND

7.1.1 See also

Concepts

SWD timing requirements on page 7-3.

7.2 SWD timing requirements

The functionality supports a *Serial Wire Debug* (SWD) connection to the *Debug Access Port* (DAP). SWD is an alternative protocol to JTAG for connecting to CoreSight processors, and has the advantage of requiring fewer pins than previous probes. It also supports higher data rates.

RealView[®] ICE connects to the serial wire-enabled target using the *Low Voltage Differential Signaling* (LVDS) probe. The interface uses only two lines, but for clarity the diagrams shown in the following figure separate the SWDIO line to show when it is driven by either the RealView ICE probe or target.

Read cycle
RVI Probe output to SWDIO Stop Park
RVI Probe output to SWDCLK
Target output to SWDIO Tri-State Tri-State Tri-State Tri-State Tri-State
Write cycle
RVI Probe output to SWDIO Stop Park
RVI Probe output to SWDCLK
Target output to SWDIO Tri-State Tri-State Tri-State Tri-State Tri-State Tri-State Tri-State Tri-State Tri-State

Figure 7-1 SWD timing diagrams

The probe outputs data to SWDIO on the falling edge of SWDCLK. The probe captures data from SWDIO on the rising edge of SWDCLK. The target outputs data to SWDIO on the rising edge of SWDCLK. The target captures data from SWDIO on the rising edge of SWDCLK.

The following table shows the timing requirements for the SWD.

Table 7-2 SWD timing requirements

Min		
	Мах	Description
10ns	500µs	SWDCLK HIGH period
10ns	500µs	SWDCLK LOW period
-5ns	5ns	SWDIO Output skew to falling edge SWDCLK
4ns	-	Input Setup time required between SWDIO and rising edge SWDCLK
1ns	-	Input Hold time required between SWDIO and rising edge SWDCLK
	10ns -5ns 4ns	10ns 500μs -5ns 5ns 4ns -

7.2.1 See also

Concepts

• *Target interface* on page 7-2.